CLAIMS

1. For a system that includes a device under test and that includes an emulator device:

a) emulating the functions of said device under test by operating in lock-step fashion with said device under test; and

b) performing a sleep operation, comprising:

b1) upon receiving a first signal that indicates that a sleep function is to be performed, initiating said sleep function at said device under test;

b2) turning off one or more clock of said device under test; and

b3) discontinuing execution of instructions that are performed in lock-step by said emulator device upon turning off said clock.

2. The method of Claim 1 wherein said clock comprises an internal CPU clock.

3. The method of Claim 2 wherein said first signal is generated by said device under test and is transmitted internally to a register that indicates that a sleep function is to be performed.

4. The method of Claim 1 further comprising:

when said sleep function has been completed by said device under test, turning on said clock and sending a second signal from said device under test to said emulator device;

receiving said second signal at said emulator device;

determining the number of clock signals received at said emulator device since said second signal was received; and

resuming execution of said instructions that are performed in lock-step at said emulator device when said determined number of clock signals received at said emulator device since said second signal was received equals a predetermined value.

5. The method of Claim 4 wherein said device under test further comprises a microcontroller and wherein said first signal comprises a first bit, said first bit received at a register of said microcontroller to indicate that a sleep function is to be performed.

6. The method of Claim 5 wherein said emulator device further comprises a Field Programmable Gate Array (FPGA) device.

7. For a system that includes a device under test and that includes an emulator device:

a) emulating the functions of said device under test by operating in lock-step fashion with said device under test; and

b) performing a stall operation, comprising:

b1) said device under test conveying clock signals to said emulator device;

b2) upon receiving a first signal that indicates that a stall function is to be performed, initiating said stall function at said device under test;

b3) upon receiving said first signal, discontinuing said sending of said clock signals from said device under test to said emulator device; and

b4) discontinuing execution of said instructions that are performed in lock-step at said emulator device while said sending of said clock signals is discontinued.

8. The method according to claim 7 wherein said device under test is a microcontroller and wherein said emulator device includes a field programmable gate array (FPGA), said clock signals further comprising signals from said microcontroller central processing unit clock.

9. The method of Claim 8 further comprising:

resuming sending of said clock signals from said device under test to said emulator device when said stall function has been completed by said device

under test, said emulator device operable upon receiving said clock signals to resume execution of said instructions that are performed in lock-step.

10. A method for performing a sleep operation, comprising:

executing a sequence of instructions by a device under test, said device under test including at least one clock for generating clock signals;

executing said sequence of instructions by an emulator device emulating the functions of said device under test, said emulator device executing said sequence of instructions in lock-step fashion with said device under test;

receiving a first signal at a register of said device under test that indicates that a sleep function is to be initiated;

initiating said sleep function at said device under test upon receipt of said first signal;

turning off said at least one clock of said device under test; and

discontinuing execution of instructions that are performed in lock-step by said emulator device upon said turning off of said clock.

11. The method according to claim 10 wherein said device under test is a microcontroller and wherein said emulator device includes a field programmable gate array (FPGA).

12. The method of Claim 11 wherein said at least one clock includes a microcontroller CPU clock.

13. The method of Claim 12 further comprising:

when said sleep function has been completed by said device under test, resuming generation of clock signals at said device under test and coupling said clock signals to said emulator device;

when said sleep function has been completed by said device under test, sending a second signal from said device under test to said emulator device;

receiving said second signal at said emulator device;

determining the number of clock signals received at said emulator device since said second signal was received; and

resuming execution of said instructions that are performed in lock-step at said emulator device when said determined number of clock signals received at said emulator device since said second signal was received equals a predetermined value.

14. The method according to claim 13 wherein said device under test is a microcontroller and wherein said emulator device includes a field programmable gate array (FPGA).

15. The method of Claim 14 wherein said first signal is a first bit, said sleep function initiated upon the receipt of said first bit at a register of said microcontroller.

16. A method for performing a stall operation, comprising:

executing a sequence of instructions by a device under test;

executing said sequence of instructions by an emulator device emulating the functions of said device under test, said emulator device executing said sequence of instructions in lock-step fashion with said device under test;

said device under test sending clock signals to said emulator device;

receiving a first signal at a register of said device under test that indicates that a stall function is to be initiated;

initiating said stall function at said device under test upon receipt of said first signal;

discontinuing said sending of said clock signals from said device under test to said emulator device upon initiation of a stall function at said device under test; and

discontinuing execution of said sequence of instructions at said emulator device while said sending of said clock signals is discontinued.

17. The method according to claim 16 wherein said device under test is a microcontroller and wherein said emulator device includes a field programmable gate array (FPGA).

18. The method according to Claim 17 wherein said clock signals further comprise signals from a central processing unit clock of said microcontroller.

19. The method of Claim 18 further comprising:

resuming sending of said clock signals from said device under test to said emulator device when said stall function has been completed by said device under test, said emulator device operable upon receiving said clock signals to resume execution of said sequence of instructions.

20. The method of Claim 19 wherein said sequence of instructions comprises the core processing functions of said microcontroller.

21. An in-circuit emulation system comprising:

a device under test that executes a sequence of instructions, said device under test operable upon receiving a first signal to initiate a stall function;

an emulator device for emulating the functions of said device under test so as to execute said sequence of instructions in lock-step fashion with said device under test, said emulator device receiving clock signals send from said device under test; and

wherein said device under test sends clock signals to said emulator device, said device under test operable upon receiving said first signal to discontinue sending said clock signals to said emulator device, said emulator

device is operable to discontinue execution of said sequence of instructions while said sending of said clock signals is discontinued.

22. The in-circuit emulation system of Claim 21 wherein said device under test is a microcontroller, said microcontroller operable to resume sending said clock signals to said emulator device when said stall function has been completed by said microcontroller, said emulator device operable upon receiving said clock signals to resume execution of said sequence of instructions.

23. The in-circuit emulation system of Claim 22 wherein said clock signals further comprise signals from a central processing unit clock of said microcontroller.

24. The in-circuit emulation system of Claim 23 wherein said emulator device comprises a field programmable gate array (FPGA).

25. An in-circuit emulation system comprising:

a device under test that executes a sequence of instructions, said device under test operable upon receiving a first signal to initiate a sleep function at said device under test and operable turn off a clock of said device under test; and

an emulator device for emulating the functions of said device under test so as to execute said sequence of instructions in lock-step fashion with said device

under test, said emulator device operable upon turning off said clock to discontinue execution of said sequence of instructions at said emulator device.

26. The in-circuit emulation system of Claim 25 wherein said device under test comprises a microcontroller, said device under test operable when said sleep function has been completed by said device under test to turn on said at least one clock and to send a second signal to said emulator device, said emulator device operable upon receiving said second signal to determine the number of clock signals received at said emulator device since said second signal was received and said emulator device operable to resume execution of said sequence of instructions when said determined number of clock signals received at said emulator device since said second signal was received equals a predetermined value.

27. The in-circuit emulation system of Claim 26 wherein 22 device under test is a microcontroller, said at least one clock further comprising a central processing unit clock of said microcontroller.

28. The in-circuit emulation system of Claim 27 wherein said emulator device comprises a field programmable gate array (FPGA).